PITT STREET RESEARCH

Revasum Inc.

Right products at the right time

Share Price: A$1.49

ASX: RVS

Sector: Semiconductor Equipment

3 September 2019

Revasum Inc. (ASX:RVS) provides grinding, polishing and CMP equipment to semiconductor substrate and device manufacturers. With the ongoing proliferation of electronics in our everyday lives, the need for semiconductor devices will continue to grow globally. As manufacturers continue to build capacity, demand for RVS' tools will grow in tandem.

Investment case: Strong focus and new products to drive high margin revenues

Compared with omnipresent 300mm wafers, the supply of ≤200mm wafers remains strained. This provides a significant opportunity for RVS, which focuses on ≤200mm wafer tools. Moreover, RVS' focus on tools for Silicon Carbide (SiC) wafers positions it very favourably to benefit from the increasing use of SiC wafers for high-growth applications, such as electric vehicles (EVs) and 5G infrastructure. As RVS continues to expand its product portfolio, with a new polisher slated to launch in 2HY19 (on 2nd October) and a new CMP tool to be introduced in 2020, we believe its growth potential is very substantial.

Cyclical upswing expected near term

Many semiconductor and equipment stocks have suffered from a cyclical downturn that started in late 2018. With the industry upcycle expected to commence in the next 6 to 9 months, RVS should witness substantial multiple expansion.

Valuation range of A$2.30–2.69 per share

We value RVS at A$2.30 per share base case and A$2.69 per share bull case (50/50 weight to DCF and peer group P/BV valuation). We believe that RVS' strong product pipeline with high Average Selling Prices and a cyclical uptick in demand will lead to significant top line growth and margin expansion.

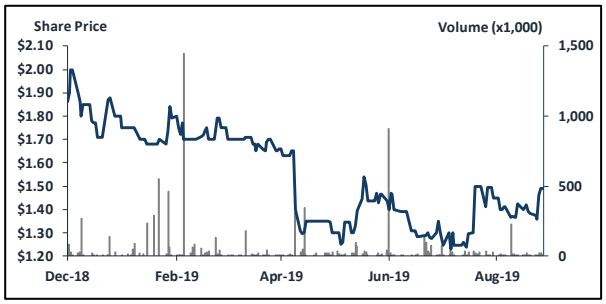
Year to June (USD)	2017A	2018A	2019f	2020f	2021f
Sales (mn)	12.5	27.3	28.2	39.6	54.7
EBITDA (mn)	-3.1	0.8	-2.5	4.0	9.9
Net Profit (mn)	-3.8	0.0	-4.2	2.1	7.2
Adj. EBITDA Margin (%)	nm	3.0%	na	10.2%	18.1%
RoA (%)	nm	nm	nm	4.3%	12.3%
EPS before extr. & amort.	-7.67	0.00	-0.06	0.03	0.09
EPS	-7.67	-0.67	-0.06	0.03	0.09
EV/Sales	0.0x	2.7x	2.5x	1.8x	1.3x
EV/EBITDA	0.0x	87.5x	-28.1x	17.6x	7.3x
P/E	0.0x	nm	nm	37.0x	10.7x

Source: Revasum, Pitt Street Research

Market Cap. (A$ m)	114.5
# shares outstanding (m)	76.6
# share fully diluted	94.1
Market Cap Ful. Dil. (A$ m)	140.2
Free Float	82.2%
6 months high/low	2.00 / 1.22
1 / 3-month performance	-0.7% / -2.0%
Website	www.revasum.com

Source: Revasum, Pitt Street Research

Share price (A$) and avg. daily volume (k, r.h.s.)



Source: Thomson Reuters, Pitt Street Research

Valuation metrics	
Fair valuation range (A$)	2.30-2.69
WACC	11.9%
Assumed terminal growth rate	2.0%

Source: Pitt Street Research

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Analyst: Marc Kennis

Tel: +61 (0)4 3483 8134

marc.kennis@pittstreetresearch.com

Profit & Loss ($m)	2017A	2018A	2019F	2020F	2021F	2022F	2023F
Sales Revenue	**12.5**	**27.3**	**28.2**	**39.6**	**54.7**	**72.9**	**86.1**
Operating expenses	-7.2	-9.6	-12.3	-12.4	-14.5	-16.5	-17.6
Adjusted EBITDA	**-3.1**	**0.8**	**-2.5**	**4.0**	**9.9**	**17.4**	**24.0**
Depn & Amort	-0.5	-0.3	-1.0	-1.2	-1.6	-2.2	-2.6
Adjusted EBIT	**-3.6**	**0.5**	**-3.5**	**2.8**	**8.3**	**15.2**	**21.5**
Net Interest	0.0	-0.3	0.3	0.0	0.1	0.1	0.1
Profit before tax (before exceptional)	**-3.8**	**0.0**	**-4.2**	**2.1**	**7.2**	**13.8**	**19.8**
Tax expense	0.0	0.0	0.0	0.0	0.0	-1.4	-4.0
Abnormal + Minorities	0.0	-4.3	0.0	0.0	0.0	0.0	0.0
NPAT	**-3.8**	**-4.4**	**-4.2**	**2.1**	**7.2**	**12.4**	**15.8**

Cash Flow ($m)	2017A	2018A	2019F	2020F	2021F	2022F	2023F
Profit after tax	-3.8	-4.4	-4.2	2.1	7.2	12.4	15.8
Depreciation	0.5	0.3	1.0	1.2	1.6	2.2	2.6
Change in trade and other receivables	-1.1	-5.7	0.8	-3.0	-3.9	-4.7	-3.5
Change in trade payables	0.8	3.5	-0.5	2.2	3.3	3.6	2.6
Other operating activities	-0.9	-1.7	-4.9	-0.2	-3.5	-3.8	-2.6
Operating cash flow	**-4.5**	**-7.9**	**-7.7**	**2.3**	**4.7**	**9.7**	**15.0**
Capex (- asset sales)	-0.2	-1.7	-9.3	-4.0	-5.5	-7.3	-8.6
Other investing activities	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Investing cash flow	**-0.2**	**-1.7**	**-9.3**	**-4.0**	**-5.5**	**-7.3**	**-8.6**
Dividends	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Equity raised (repurchased)	4.8	25.3	0.0	0.0	0.0	0.0	0.0
Debt drawdown (repaid)	1.0	6.5	2.0	0.4	-0.9	-0.5	0.0
Other financing activities	-0.1	-0.1	0.0	0.0	0.0	0.0	0.0
Net change in cash	**1.0**	**22.1**	**-15.0**	**-1.2**	**-1.7**	**1.9**	**6.4**
Cash at End Period	2.4	24.5	9.4	8.2	6.5	8.4	14.8
Net Debt (Cash)	-1.4	-24.5	-7.4	-5.8	-5.0	-7.4	-13.8

Balance Sheet ($m)	2017A	2018A	2019F	2020F	2021F	2022F	2023F
Cash	2.4	24.5	9.4	8.2	6.5	8.4	14.8
Total Assets	10.2	44.2	42.5	47.9	58.6	75.6	95.8
Total Debt	1.0	0.0	2.0	2.4	1.5	1.0	1.0
Total Liabilities	7.3	9.2	10.7	13.3	15.7	18.8	21.4
Shareholders' Funds	2.9	35.0	31.8	34.6	42.9	56.8	74.4

Ratios	2017A	2018A	2019F	2020F	2021F	2022F	2023F
Net Debt/Equity (%)	nm	nm	nm	nm	nm	nm	nm
Interest Cover (x)	nm	2.0	nm	nm	nm	nm	nm
Return on Equity (%)	nm	nm	nm	6.0%	16.8%	21.8%	21.3%

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Investment Case: Strong focus and new products to drive high-margin revenues

Revasum (RVS) manufactures polishing, grinding and chemical mechanical planerisation (CMP) equipment for semiconductor substrate and device manufacturers. Its tools play a critical role in improving the yield and performance of a semiconductor manufacturing line.

We believe that RVS is an attractive investment proposition:

- **Constrained supply of new equipment for the smaller wafer segments:** Although the global silicon (Si) wafer industry is dominated by 300mm wafers, wafer sizes of ≤200mm will continue to hold relevance among manufactures due to numerous end-market applications, such as power electronics, 5G infrastructure, automotive and Internet of Things (IoT) devices. We expect the supply of new tools to process 200mm substrates and devices to remain constrained in the medium term.
- **Growing demand for SiC wafers:** Si is currently the most used material in 200mm wafer manufacturing. However, SiC gradually is becoming the material of choice for high-performance Integrated Circuits (ICs) due to its superior qualities, including high thermal conductivity and the ability to operate at high voltages and temperatures. While the market for Si wafers will continue to be bigger than that of SiC, the SiC wafer market is anticipated to grow exponentially in the next few years. The key application areas for SiC wafers will be high-priced power electronics, especially for electric vehicles (EVs) and 5G infrastructure.
- **Well poised to capitalise on industry trends:** RVS is in a highly favourable position to benefit from the abovementioned trends due to its focus on producing equipment for ≤200mm SiC wafers. Furthermore, RVS specialises in tools for single-wafer processing which is more precise and safer than batch processing and hence more suitable for SiC wafers.
- **Specialised nature of RVS' offerings give it an edge over competitors**: RVS is focusing on a segment that is not properly addressed by the larger players that are mainly focusing on equipment for 300mm wafers, Si wafers and/or batch processing. Niche players such as RVS have an advantage in catering to a specific target market with specialised offerings. RVS offers the widest product range among its direct competitors across grinding, polishing and CMP equipment. Additionally, RVS' technology enjoys IP protection with the company holding ~63 active US patents.
- **New product launches:** RVS has a strong balance sheet that will support its strategy to launch multiple new products over the next 3-5 years. The company is aiming to start shipment of its new single wafer SiC polishing tool in 2HY19. The new 200mm CMP tool for Si-based applications is expected to commence shipping in 2HY20. This tool will be a potential steppingstone to a 300mm tool.
- **Attractive valuation:** We believe there is substantial upside to RVS' share price given its top-line growth prospects (driven by higher ASP's for new products), margin expansion and the expected upswing in the semiconductor industry from 2HY19 onwards. Also, we expect strong multiple (P/BV) expansion for semiconductor and equipment companies when this industry upswing materialises, further contributing to RVS' attractiveness at current share price levels.

  Our valuation range for RVS is A$2.30 to A$ 2.69 per share.

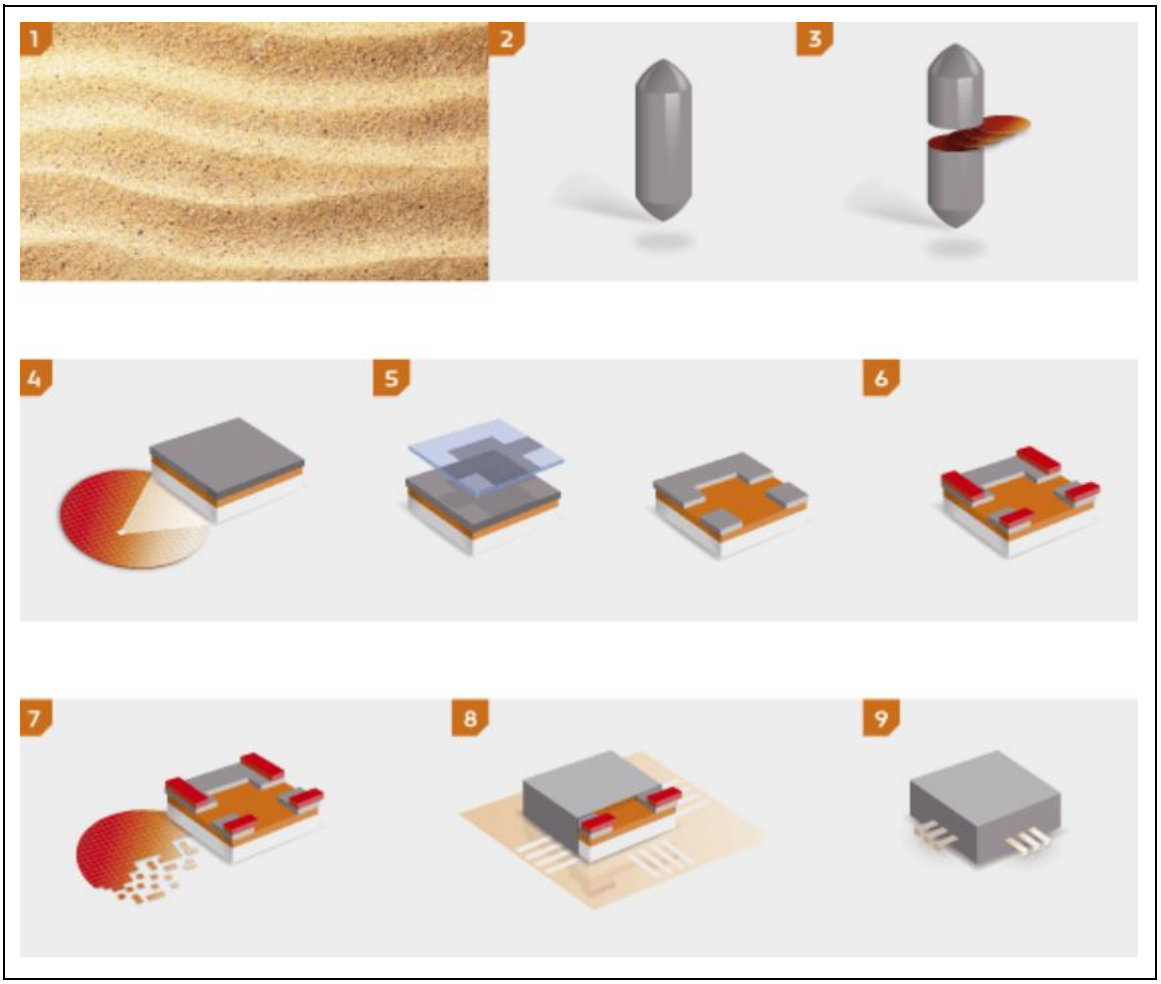
Semiconductor manufacturing 101

A semiconductor chip is also known as an Integrated Circuit (IC) or die

Before we get into the specifics of RVS as a company, its products and its target markets, let's first have a look at how computer chips, or semiconductors, Integrated Circuits, or die, are manufactured.

The first step (Figure 1) for any silicon-based IC, or chip, is to take common sand and purify the silicondioxide (SiO_2) in sand to get pure silicon (Si) (step 1). When we say pure, we mean only one foreign atom for every billion silicon atoms.

Figure 1: How semiconductors are manufactured



Source: ASM International

The pure, mono-chrystalline silicon is melted at 1,420 degrees centigrade and grown into a silicon ingot (step 2) over a period of several weeks. The ingot is then sliced up into individual raw wafers, or substrates, (step 3) that are roughly 0.2 millimeters (200 microns) in thickness.

The most common Si wafer diameters today are 200 millimeter (mm) and 300mm; however wafers with diameters of 50mm, 75mm, 100mm and 150mm are still prevalent in compound semiconductor manufacturing (Figure 2).

Figure 2: Raw semiconductor wafers of different sizes

Source: Samsung

An insulating silicondioxide layer is grown to prevent leakage of electrical charges

Before the actual chip circuitry can be patterned, oxygen is used to grow a SiO_2 layer on top of the wafers (step 4), which acts as an insulating layer against leakage of electrical charges and currents.

Epitaxial wafers and SiC

In addition to a SiO_2 layer, an epitaxial layer is often grown on wafer surfaces, especially on wafers for high-performance semiconductors, such as SiC.

The word epitaxy comes from the Greek epi meaning "above", and taxis meaning "in an ordered manner". The process of manufacturing an epitaxial wafer is known as epitaxy, which involves the deposition of Si or Si compounds on a bare Si wafer to form layers that help to perfect the crystal structure (**Error! Reference source not found.**).

Epitaxy is used in semiconductor fabrication either to create a perfect crystalline foundation layer or to alter attributes of a bare wafer in a way that improves its electrical conductivity. The other benefits of epitaxy include low noise performance (low emission of unwanted electrical signals) and the capability to handle higher power levels. Hence, epitaxy has become an essential process for building semiconductor components for high-performance power and RF devices.

SiC and Gallium Nitride (GaN), owing to their superior properties, are preferred compounds for use in building wafers with epitaxial layers. It is the SiC/GaN-based epitaxial layer that determines performance uniformity and yield of transistors and diodes formed on the wafer.

There are two different types of epitaxial wafers, thin and thick. Thin epitaxial wafers are commonly used for metal-oxide semiconductor (MOS) devices. Thick epitaxial or multi-layered epitaxial wafers are used for devices that control electric power. The thickness and doping[1] concentration of

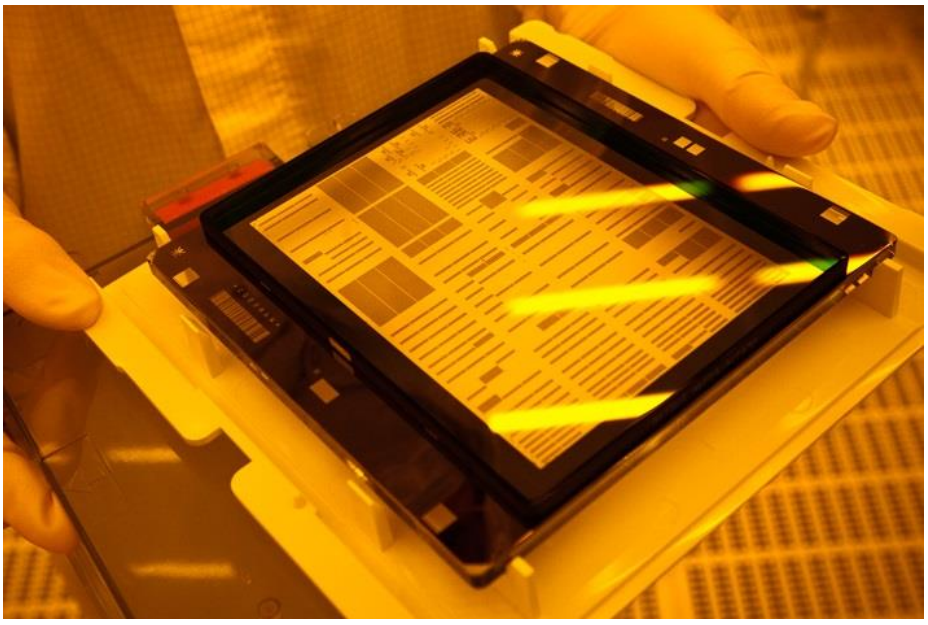
[1] Doping refers to the selective control of the conductivity of the material. In doped semiconductors, the conductivity is improved through incorporation of foreign atoms.

epitaxial layers grown on SiC wafers require very high process control and hence, single wafer processing is highly suitable for SiC wafers. This bodes well for RVS' products with the company's focus on supporting single wafer SiC processing.

Transferring the chip design onto a wafer

An individual chip consists of many layers, depending on the complexity of design and application. Each layer requires a so-called photomask (step 5) that holds the design of that particular layer (Figure 3). A mask set with photomasks for all the layers for complex logic semiconductors, such as central processing units (CPUs), typically costs several millions of dollars.

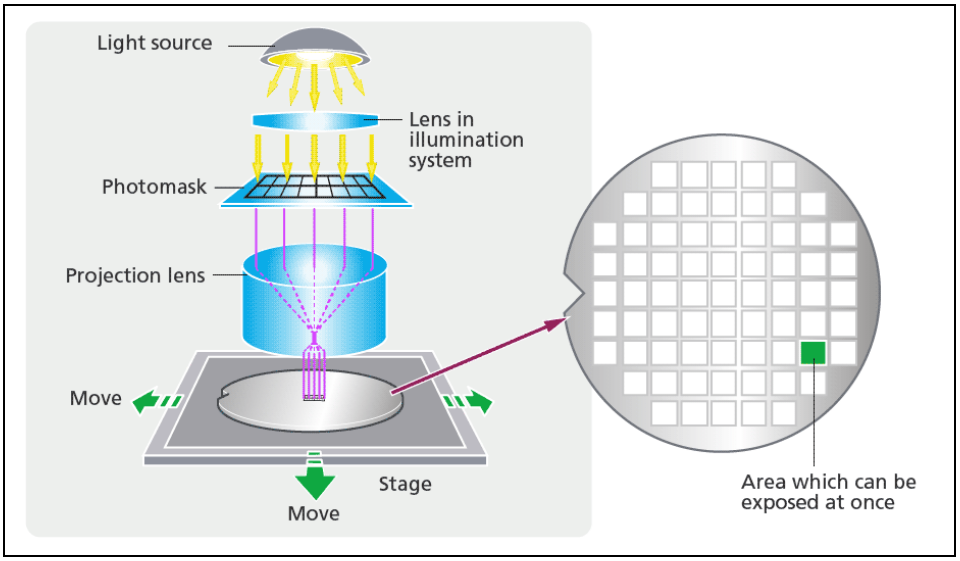
Figure 3: Photomask of one layer of circuitry for an individual chip



Source: Intel

Transferring the circuitry design of one layer of the chip from the photomask onto the wafer (step 6) is carried out through a process called lithography, which is somewhat similar to transferring a slide's image onto a white screen using a slide projector. Prior to this step, the wafer is coated with photoresist, a light-sensitive material that reacts and hardens when exposed to (extreme) ultraviolet (UV) light, the kind used in the lithography process (Figure 4).

Figure 4: Transferring the circuitry onto the wafer using lithography

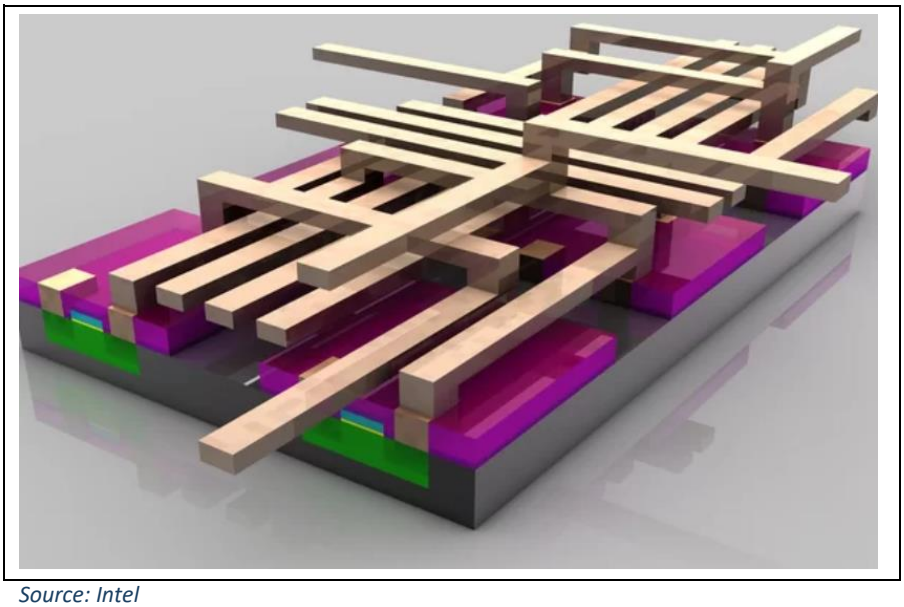


Source: Nikon

Lithography is the most crucial step in the manufacturing process

In the lithography process, UV light is flashed through a system of lenses and through the photomask, in order to transfer the circuitry pattern onto the wafer. The exposed areas are developed and etched away, leaving a trench. Either a conductive or insulating material can subsequently be deposited into these trenches, creating the circuitry of the chip. As many as 400 to 600 process steps may be required to create a fully functional chip (Figure 5).

Figure 5: Look-through of the chip circuitry once finished



Source: Intel

Once this front-end process is completed, the individual chips are cut out of the wafer (step 7) and placed on carriers, and electrical connections (step 8) are prepared to connect the chips to the outside world later on, e.g., when placed on printed circuit boards. The final step is to cover the chip in a protective epoxy (step 9).

While the front-end process is performed by integrated device manufacturers (IDMs), e.g., Intel, NXP and Samsung, as well as semiconductor foundries such as TSMC and SMIC, these back-end process steps of dicing, wiring and packaging are typically performed by specialised back-end assembly companies.

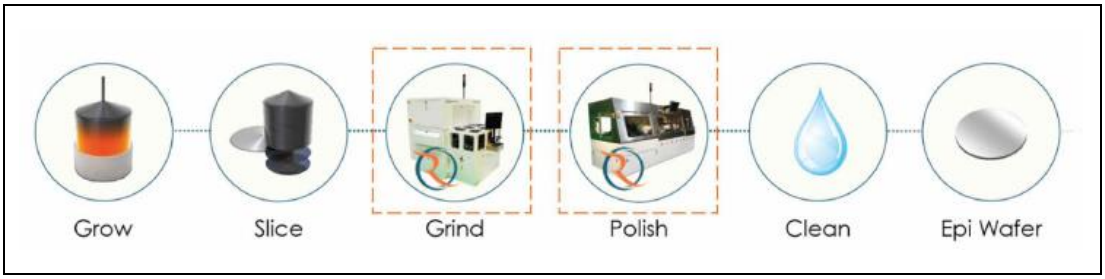
With respect to the above semiconductor manufacturing process, Revasum provides polishing, grinding and chemical mechanical planerisation (CMP) equipment used to smooth the surface of newly fabricated wafers (after step 3) and to even out the wafer surface after deposition of materials (part of step 6).

Revasum provides polishing, grinding and CMP tools

Polishers and grinders are used in substrate manufacturing

The semiconductor manufacturing equipment RVS provides, specifically grinders and polishers, is used to flatten and smooth the surface of semiconductor substrates after they have been sliced out of the ingot (Figure 6).

Figure 6: RVS equipment used in the substrate manufacturing process (step 3 in Figure 1)

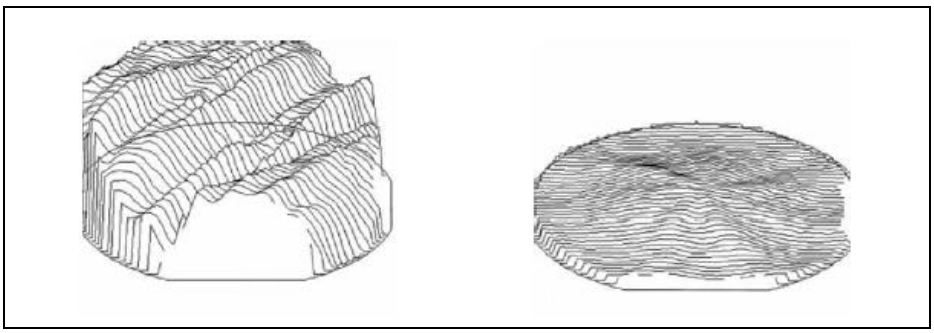


Source: Revasum

Die yield: The percentage of chips in a finished wafer that pass all tests and function properly

The surface of newly sliced wafers is typically very uneven and damaged (Figure 7) due to the slicing process, and this affects yield. Die yield is the percentage of chips in a finished wafer that pass all tests and function properly.

Figure 7: Silicon substrate before (left) and after grinding



Source: Revasum

Grinding and polishing help improve die yield further down the production line

Given that the size of the electronic circuitry that is to be manufactured on top of the substrate is very small, i.e., measured in nanometers (1 nanometer = 1 millionth of a millimeter), the substrate needs to be extremely smooth before any further processing can be done. Moreover, grinding the substrates also ensures an optimal substrate thickness with minimal variations across the substrate area.

Once grinded down, substrates are subsequently polished to further smoothen the surface, which improves die yield further, leading to fewer defective ICs per wafer at the end of the manufacturing process.

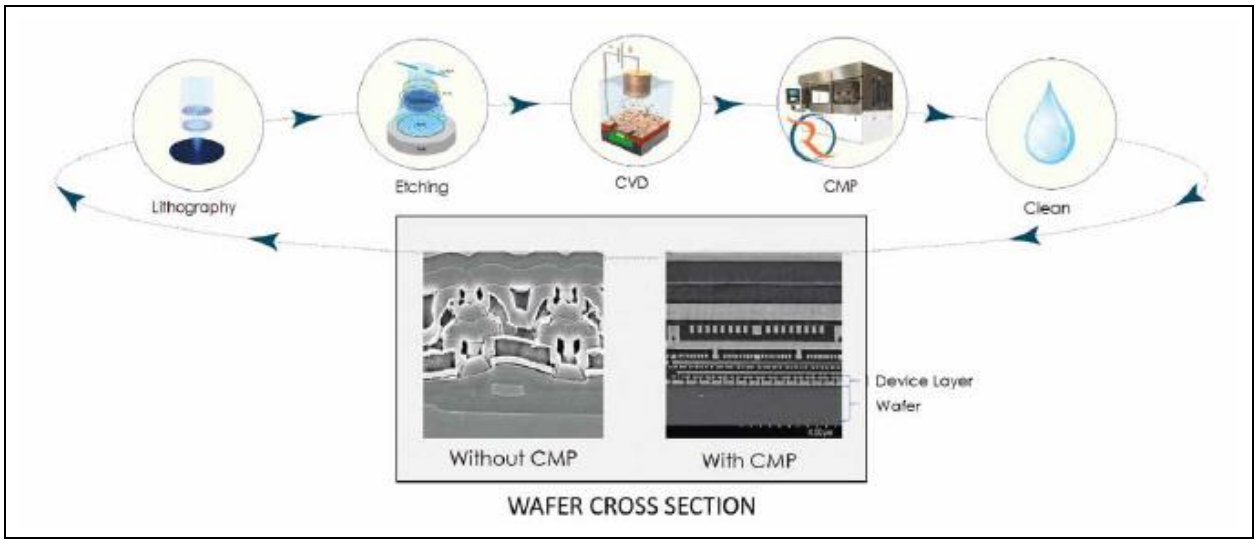
Yield is the single most important yardstick for semiconductor manufacturers when evaluating an individual production line. The higher the yield, the higher the revenue and margin from the particular type of chip that is manufactured on that line. Yield is influenced by a number of aspects, including contamination, operator performance, chip design margins and process uniformity, or lack thereof.

CMP tools are used in the chip manufacturing process

Chemical mechanical planerisation (CMP) is a polishing process assisted by chemical reactions to remove excess surface materials, such as conductive and dielectric (insulating) materials, that are deposited on the wafer surface (Figure 8).

Similar to grinding and polishing of substrates, the aim of the CMP step in the semiconductor manufacturing process is to create a near-perfect flat and smooth surface in preparation for the next process step.

Figure 8: RVS equipment used in the semiconductor manufacturing process



Source: Revasum

Revasum's strategic advantages

1. Single-wafer processing

Single-wafer processing has several key advantages

RVS is one of the very few companies that manufacture grinding and polishing equipment for single-wafer processing, i.e., processing of a single wafer at a time. The alternative is batch processing, in which a dozen or more wafers can be polished simultaneously, depending on the wafer size (the smaller the wafer, the higher the throughput).

Batch processing is less precise and increases the risk of damaging wafers

The major benefit of batch processing is high throughput, i.e., the number of wafers that can be processed in any given period of time. High throughput lowers the processing costs per wafer. However, batch processing can impact yield as there is less process control over individual substrates being processed in a particular batch; specifically, there is typically less thickness uniformity from one substrate to the next.

Additionally, the loading and unloading of wafers is a manual and dirty process, given the slurry involved. This increases the risk of damaging the substrates that are processed in batches.

Single-substrate processing particularly relevant for SiC wafers

RVS' grinding and polishing tools for single-substrate processing allow for very high process consistency across large numbers of substrates and therefore enable very high uniformity from substrate to substrate.

RVS' grinding tools for SiC substrates achieve a thickness variation of less than 2 microns (1 micron = 1 thousandth of a millimeter), while typical batch grinding tools only guarantee thickness variation of less than 10 microns.

Additionally, RVS' single-wafer process is entirely automated from start to finish, including substrate cleaning, resulting in fewer incidents of substrate damage. This inceases yield across the production line.

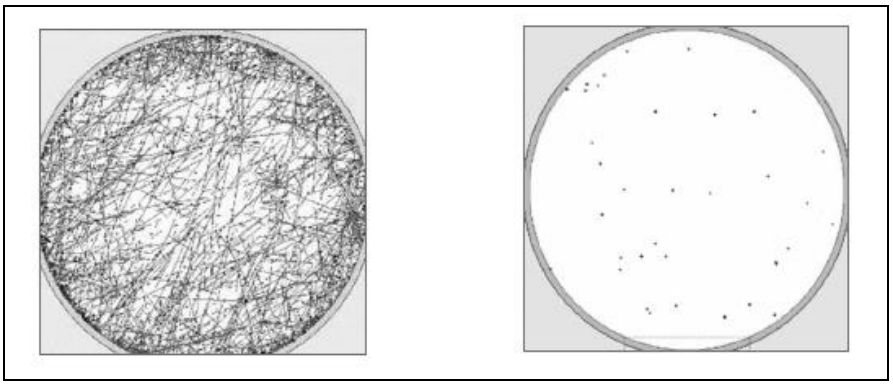
SiC substrates are a lot harder than Si substrates

Apart from high substrate-to-substrate uniformity, the proliferation of SiC substrates, which we will discuss later, is driving the need for single-substrate processing to remove wire saw damage and prepare substrates for deposition of materials to grow the epitaxial layer of the substrates.

Given the carbon element in SiC substrates, the material is much harder than SiO_2 substrates, which is very challenging for batch processors.

Figure 9 illustrates the difference between a batch polisher that uses a diamond abrasive and RVS' single-wafer poslisher for SiC wafers. Batch polishing in this sample resulted in ~20,000 scratches post polish versus zero scratches in RVS' single-wafer polisher.

Figure 9: SiC batch processing (left) vs. RVS' SiC single-wafer polishing



Source: Revasum

2. Servicing the ≤ 200mm wafer market

Most of the industry's R&D budget is spent on developing 300mm equipment

Most high-volume manufacturing these days is done on 300mm wafer sizes as this gives IDMs a substantial cost advantage (~30% cheaper per chip than manufacturing on 200mm wafers). Consequently, most R&D dollars for semiconductor manufacturing equipment are spent on developing tools to process 300mm wafers, including polishing, grinding and CMP tools.

Not only has this created a significant shortage of systems for substrate and device manufacturing at ≤200mm, it has also resulted in a lack of innovation for smaller wafer sizes by semiconductor equipment companies. Hence, by continued innovation in tools for 150mm and 200mm substrates, we believe RVS has created an attractive market opportunity for itself.

Larger players, such as Applied Materials (NASDAQ:AMAT), are not strategically focussed on 200mm and smaller wafer sizes, and only service this market segment by providing refurbished tools. While this does not mean that none of the larger players will enter the ≤200mm tool market at some point, we believe RVS is well-positioned to succesfully defend this market niche going forward.

RVS' product suite currently focused on ≤200mm wafer sizes

RVS' current product portfolio (Figure 10) addresses the market for grinders, polishers and CMP tools for wafer sizes from 50mm to 200mm, even though the bulk of revenue is derived from 150mm and 200mm equipment.

Figure 10: RVS equipment used in the substrate manufacturing process

Product		Market	Primary applications	Wafer sizes
6EC-II		Device	Low-volume production applications, thin film CMP and consumables or process R&D	75-200mm
6DS-SP R		Device & substrate	High-volume production for the thinning of film CMP and the polishing of SiC substrates	100-200mm
6DZ-II		Substrate	High-volume Si substrate polishing	100-200mm
7AF-HMG		Device & substrate	Grinding of hard material wafers (including SiC)	50-200mm
7AF-R		Device & substrate	Thinning of Galium arsenide (GaAs), Si and Indium phosphide (InP)	50-200mm

Source: Revasum

Product roadmap to capture SiC and 300mm opportunities

The capital raised in RVS' IPO in 2018 has partly been used to refresh the company's polisher and grinder offerings, e.g., the new SiC polisher and the new CMP tool.

The new SiC polishing tool, intended to succeed the 6DS, has been in development since 2018 and is expected to start shipping in 2HY19 (to be launched on 2 October 2019). Initially, RVS expects to ship a handful of these tools to co-development customers that provided system requirements and feedback to RVS during development of the tool. However, following the initial release of the product to these early adopters, the company is anticipating strong demand for this SiC polisher.

New 200mm CMP tool is a potential stepping stone to 300mm tool

The new 200mm CMP tool, which is aimed at Si-based devices, is expected to start shipping in 2HY20. We do not expect a significant ramp-up of deliveries of this tool till the latter part of 2020.

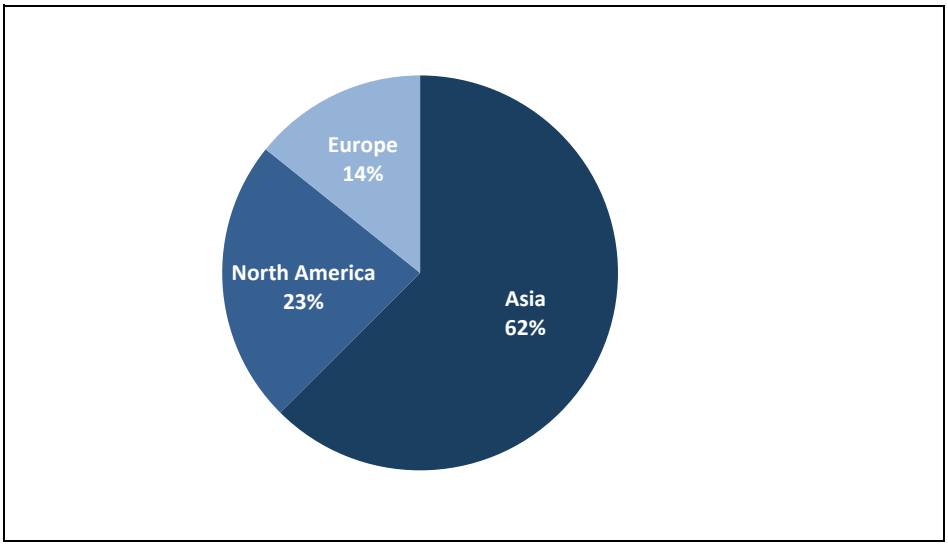
We believe the new 200mm CMP tool can potentially be a prelude to RVS' expansion into the CMP market for 300mm Si-based devices in a few years' time. Of course, this segment is currently well-served by large companies, such as Applied Materials, but RVS may leverage its specific IP portfolio in

single-wafer 200mm applications to succesfully expand into this larger wafer size.

SiC tools to diversify RVS' geographical revenue mix

Historically, the demand for RVS' tools has largely originated from Asia, primarily due to its high concentration of semiconductor manufacturers. In 2018, Chinese semiconductor sales reached US$97.3bn, representing 20% of the global semiconductor revenue. For RVS, ~62% of the company's total revenue in FY2018 was from Asia (Figure 11).

Figure 11: Asia dominates RVS' revenue mix (FY18 data)



Source: Revasum

Growing demand for SiC tools to drive a shift in revenue mix towards US and Europe

However, as the company shifts its focus towards SiC substrates, the revenue mix for RVS is expected to get more balanced, due to the presence of high-end product manufacturers in the US and Europe. SiC tools are more used in these geographies, among other things due to the presence of IDM's focussed on Automotive semiconductors and the support from the respective governments. For instance, under the US Department of Energy's CIRCUITS programme, the government has announced to invest US$30m to fund 21 projects for the development of power converters based on wide bandgap semiconductors, which are based on SiC substrates. Similarly, the EU has adopted a Strategic Action Plan for Batteries in May 2018 for the purpose of building a battery value chain in Europe.

As these initiatives take-off, the demand for SiC wafers is anticipated to grow across Europe and the US, which will help RVS have more of a balanced revenue mix by geography.

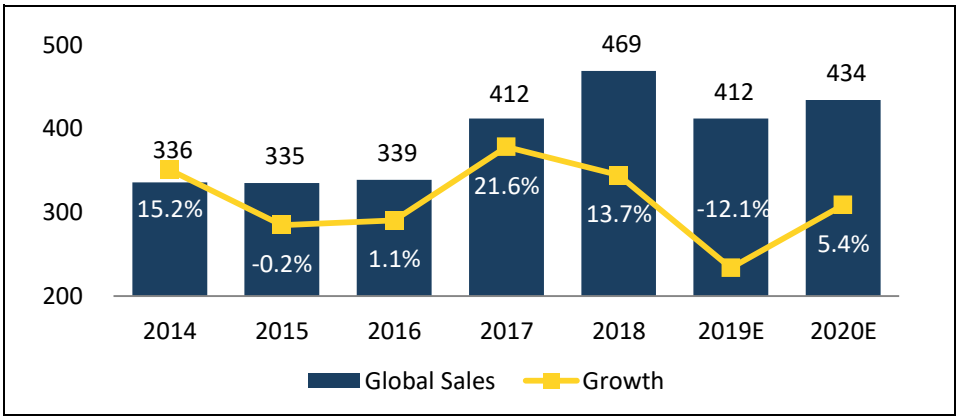
Structure and outlook of RVS' end markets

Global semiconductor sales will benefit from diverse growth drivers, such as rise in use of smartphones, IoT-enabled devices and automotive components

All modern electronic equipment these days, including smartphones, laptops, tablets, Internet of Things (IoT)-enabled devices and automotive components, are created using semiconductor devices. This has led to expansion in the global semiconductor industry, which grew at a CAGR of 10% over the past five years. The industry is further expected to grow steadily in the medium term on the back of increasing demand for automation and digitalisation.

Although World Semiconductor Trade Statistics (WSTS) projects the industry's global sales to decline 12.1% y-o-y in 2019 – due to the US–China trade war, a decline in global smartphone sales and a fall in global personal computer and laptop shipments – it expects a bounce back in 2020, with a growth of over 5% in global sales (Figure 12).

Figure 12: Global semiconductor market size (US$bn)



Source: Semiconductor Industry Association (SIA), WSTS Semiconductor Market Forecast Spring 2019

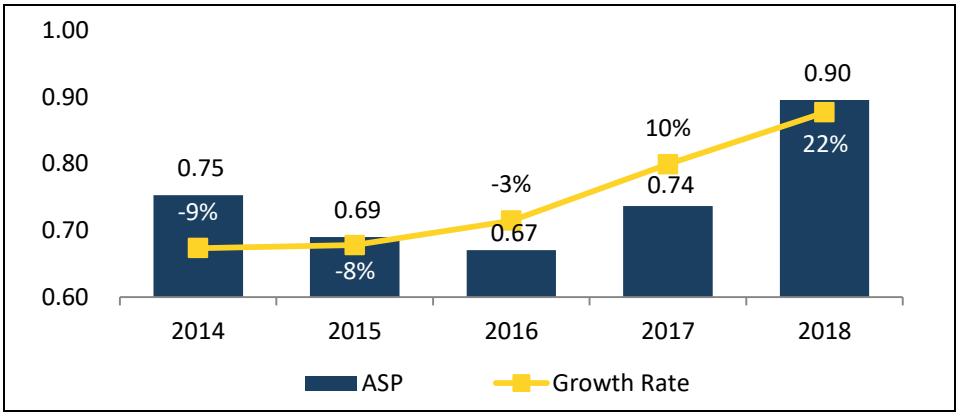
Across the semiconductor manufacturing value chain, RVS sells its equipment to both 1) substrate manufacturers that produce base wafers, which are an input for the device manufacturing process and 2) device manufacturers that build ICs and discrete devices on these substrates.

Steady growth in the Si wafer market underpinned by demand from consumer electronics and automotive sectors

Demand for Si wafers grew strongly over the past two years on the back of the flourishing IC industry

Historically, semiconductor manufacturers have had a tendency to build excess manufacturing capacity during boom times, only to find themselves competing on prices and struggling with overcapacity during down cycles. This has been especially true for manufacturers of both DRAM and flash memory. In 2016, the IC industry started flourishing again, driven by strong demand for memory products in particular, causing a spike in demand for Si wafers. At that point, there was a shortfall in capacity, specifically for 200mm and 300mm wafers, which led to increase in the prices of Si wafers (Figure 13).

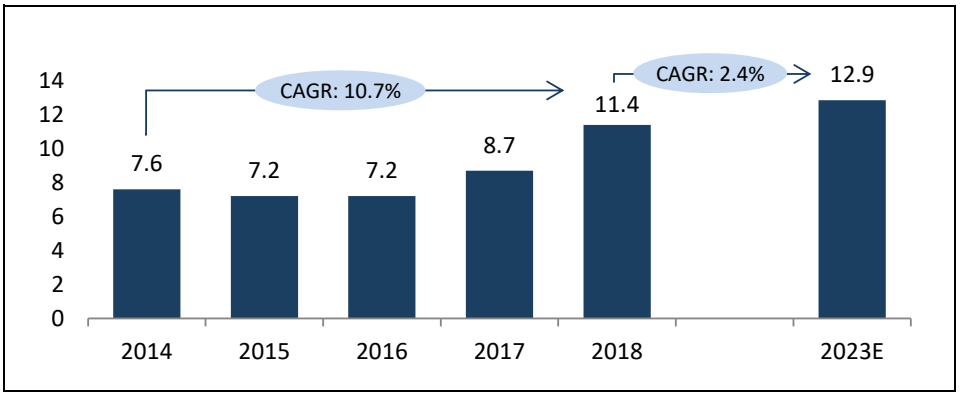
Figure 13: Average selling price of Si wafer (US$, per square inch)



Source: SEMI

Consequently, between 2016 and 2018, Si wafer revenues grew at a CAGR of ~26% to reach US$11.4bn (Figure 14). Rising demand for consumer electronics – and hence memory and storage capacity – combined with advancements in electric vehicles (EVs) and growth in IoT devices, has supported demand growth for Si wafers in the past few years. As substrate and IC manufacturers gear up to meet the growing demand, the need for requisite equipment, i.e. RVS' products, will also rise.

Figure 14: Global Si wafer market size (US$bn)



Source: SEMI, ResearchAndMarkets

Slowdown in late '18 and early '19, growth to resume late 2019

Driven by slowing end demand, combined with excess manufacturing capacity in the market, demand for DRAM and flash memory started to taper off in late 2018 and this has continued into 2019. According to the SIA, global semiconductor sales decreased 13% y-o-y and 15.5% q-o-q in Q1 2019. Consequently, Si wafer demand has slowed as well.

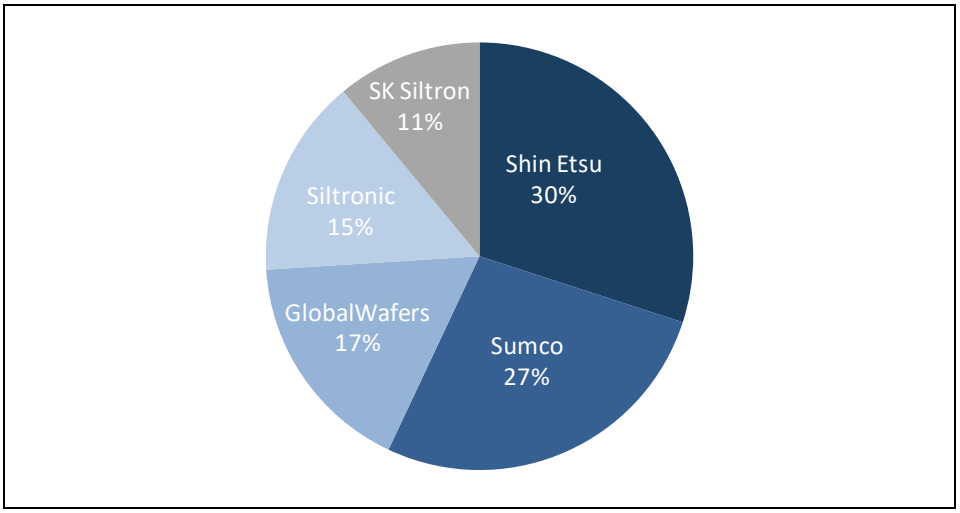
However, this slowdown in semiconductor sales is expected to be temporary, with growth expected to resume in late 2019 and 2020. The long-term outlook for the semiconductor industry, and hence wafer manufacturing capacity, is expected to remain robust due to increasing and diversified applications of semiconductor devices.

Si wafer industry is highly consolidated

The Si wafer manufacturing market, once characterised by the presence of many small players (~20 companies in 1990s), has now consolidated to just a handful of large players. As companies need a significant amount of capital to compete in the business, small players have found it difficult to sustain and eventually, over the years, have been acquired by larger companies. Notably, in 2016 alone, the industry witnessed 10 major M&A deals including the acquisition of SunEdison Semiconductor by GlobalWafers for US$683m.

Currently, the market is dominated by five large companies that control 90% of the global supply, with Japanese companies Shin-Etsu Handotai and Sumco holding the lion's share of 30% and 27%, respectively (Figure 15).

Figure 15: Si wafer production market share across all diameters (2018)



Source: Siltronic

Although 300mm dominates the market, ≤200mm wafers are vital to the industry going forward

Si wafers come in different sizes – 100mm (4 inches), 150mm (6 inches), 200mm (8 inches) and 300mm (12 inches). In 2018, 300mm wafers held a leading share of 68% in the market (Figure 16) on the back of their applications in memory (DRAM and NAND), power management devices, image sensors and personal computers, and the fact that they provide an approximate 30% cost benefit per IC manufactured on a 200mm wafer.

IHS Market estimates area shipments for 300mm Si wafers to grow at a CAGR of 4.8% from 2017 to 2022 (Figure 17), as major semiconductor manufacturers continue to build capacity in this segment to meet their needs for memory and logic applications. As large substrate suppliers are increasingly focussing on 300mm wafers, supply for 150mm and 200mm wafers – where RVS operates – is expected to remain tight in the near future.

200mm wafer size is expected to remain a significant part of the Si wafer market

While the larger 300mm chip size offers substantial economies of scale, resulting from a larger number of chips produced from a single wafer (typically 2.3x more chips on a 300mm wafer compared with a 200mm wafer), wafer sizes of ≤200mm continue to hold relevance among manufacturers. This is primarily due to the many different ICs used in areas such as power electronics, 5G infrastructure, automotive, IoT, Industry 4.0 and mobile applications, which are still manufactured using 200mm wafers.

As these underlying industries continue to grow, demand for 200mm wafers is expected to remain strong. IHS Market estimates 200mm Si wafer shipments to grow at a CAGR of 3.4% over 2017–2022.

Figure 16: Global Si Wafer Area – by Size (2018)

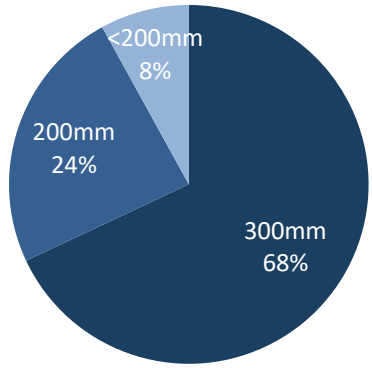
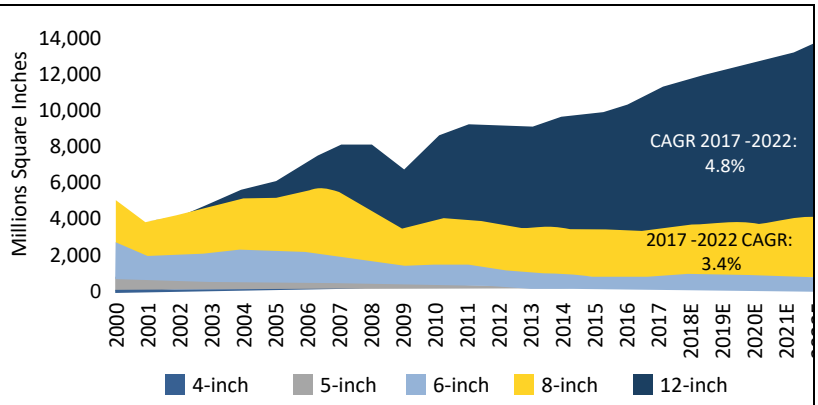


Figure 17: Global Si wafer shipments



Source: Siltronic, IHS Market, Pitt Street Research

Supply of 200mm wafers continues to remain strained, pushing wafer vendors to build capacity

The supply of 200mm Si wafers was constrained in 2018 because of the slow build-up of capacity by substrate manufacturers. However, with solid prospects for 200mm Si wafer growth, wafer manufacturers are expected to invest in capacity expansions in the medium term, once resumption of growth in semiconductor sales becomes more pronounced.

As evidenced by the 'Global 200mm Fab Outlook' report published by SEMI in January 2019, 200mm manufacturing capacity is forecast to grow substantially over the next three years, with the industry estimated to add 16 new fabs – including 14 volume fabs globally. The increase in capital outlay by semiconductor manufacturers for 200mm wafers should lead to a rise in demand for RVS' machines, in our view.

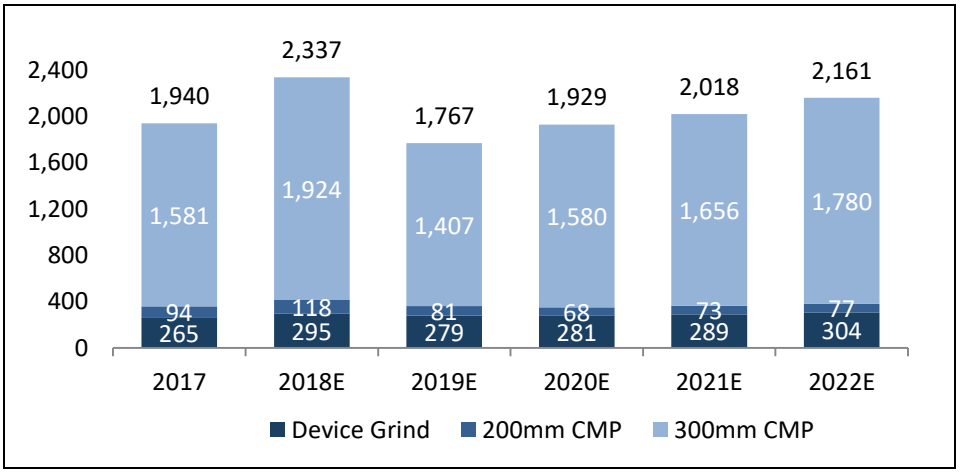
Notably, RVS currently serves 200mm and lower diameters. However, in the longer term, the company plans on addressing the 300mm segment through its new CMP system offerings, which should help it expand into the equipment market for larger wafer sizes.

Growth in semiconductor market to boost CMP and grinding capital equipment market

The CMP and grinding equipment market, which represented ~4% of the US$64.5bn semiconductor equipment market in 2018, is expected to grow through 2022, following a decline in 2019 (Figure 18). The current lull in the market is primarily driven by dip in demand for DRAM and flash memory chips as end demand has slowed down and electronics companies are looking to rationalise their inventory levels.

RVS does not currently supply to IDMs in this segment as substantially all DRAM and flash memory manufacturing is done on 300mm wafers, given the economies of scale that can be achieved by using this wafer size.

Figure 18: CMP and Grinding Equipment market size (US$m)



Source: VLSI Research, Wafer Fab Equipment Market Forecast

Growth in 200mm production to drive demand for RVS' tools

Customised wafer processing equipment for specific applications is an advantage for players such as RVS

Regarding end markets that are relevant for RVS, in 2020, a substantial uptick is expected from the automotive industry and the development of wireless infrastructure to support transition to 5G. Chips for these applications are largely still manufactured on 200mm wafers. Consequently, we expect continued demand for 200mm wafers, although the mainstay of semiconductor fab investments will be 300mm wafers going forward. 200mm wafers are expected to remain the preferred wafer size for more specialised semiconductor applications.

The semiconductor equipment market is dominated by few large players – such as Applied Materials, ASML and Lam Research – but the specific nature of wafer processing equipment demanded by IDMs for application in power management, 5G, etc., provides an advantage to niche players such as RVS, which offer specialised grinding and CMP systems for these applications. Additionally, the expected launch of RVS' new CMP system in 2020 will enable the company to address a larger portion of the overall CMP and grinding capital equipment markets.

Competition strongest in grinding and polishing

The global CMP and grinding capital equipment market is highly competitive, consisting of a large number of small players and few large players. Although a majority of companies operate in the 300mm wafer equipment domain, the market for ≤200mm equipment is expected to remain highly competitive on the back of an anticipated strong growth in end-market applications for EVs and 5G.

Figure 19 illustrates the competitive landscape for RVS for its grinding, polishing and CMP systems. It is evident that RVS has the widest product range among its direct competitors across grinding, polishing and CMP equipment.

Figure 19: RVS' competitive landscape (≤200mm wafer size)

Company Name	Process Type	Product Type			Primary Focus Area
		Grinders	Polishers	CMP Systems	
Revasum	Single Wafer	✓	✓	✓	≤200mm SiC market
DISCO	Single Wafer	✓	✓		≤300mm Si market and 200mm SiC market
ACCRETECH	Single Wafer	✓		✓	≤300mm Si market and ≤200mm SiC market
Okamoto	Single Wafer	✓	✓		≤300mm Si market and SiC market
EBARA	Single Wafer			✓	300mm wafer market
APPLIED MATERIALS make possible	Single Wafer			✓	300mm wafer market
AXUS TECHNOLOGY	Single Wafer	✓	✓	✓	3rd party reseller to Disco, Okamoto, Applied Material and G&P
G&P TECHNOLOGY	Single Wafer	✓		✓	≤300mm Si market and ≤100mm SiC market
entrepix	Single Wafer			✓	3rd party reseller to Applied Material and Speedfam
LOGITECH	Batch and Single Wafer		✓		≤150mm Si market and 100mm SiC market
PR HOFFMAN	Batch		✓		≤300mm Si market
GigaMat	Batch	✓	✓		≤300mm Si market; also provides polishers for SiC
SPEEDFAM	Batch	✓	✓		≤300mm specialty substrates including Si, metal, SiC, sapphire and oxide substrates
fujikoshi	Batch		✓		300mm Si market
LAPMASTER	Batch		✓		≤300mm Si market; also provides polishers for SiC, sapphire and gallium arsenide

Source: Revasum, Pitt Street Research

Strong competition in grinding segment

RVS faces tough competition in the grinding segment for Si wafers from Japanese players, such as DISCO Corp and Accretech, with DISCO alone holding ~80% market share. However, RVS has substantial dominance in grinders for the SiC market, specifically for wafer sizes of ≤200mm.

Notably, DISCO introduced a new laser technology for wafer slicing that makes the process more affordable for substrate manufacturers by replacing the use of diamond wire saws. Moreover, the new technology allows for high-speed production of SiC wafers, as it increases the number of wafers produced from a single ingot. This is expected to drive the acceptance of SiC as the substrate of choice among manufacturers. In our view, as more manufacturers adopt SiC as their substrate, the demand for other requisite tools to process these wafers would grow, thereby stimulating demand for RVS' grinders.

RVS not competing directly with large CMP players

Although there are several large players in the CMP systems segment, such as EBARA and Applied Materials, they are not direct competitors for RVS. EBARA has highlighted its interest in 300mm Si-based devices and announced that it will not focus on the SiC segment. Applied Materials, on the other hand, does operate in the SiC market but offers only their legacy CMP product (MIRRA series), originally designed for thin film planerisation. Applied Materials CMP system is currently facing technical problems due to the highly acidic slurries used for SiC wafers. In our view, RVS has a competitive edge in this segment due to the specialised nature of its offerings and experience in substrate manufacturing.

RVS does compete with batch manufacturers, such as PR Hoffman, Lapmaster Wolters, Speedfam and Gigamat. As batch manufacturers have throughput advantages, they pose a threat to RVS' offerings. Most 50mm, 75mm and 100mm SiC wafers are manufactured using batch lapping and polishing equipment from these companies. In our view, as the industry further transitions towards 150mm and 200mm wafer sizes, RVS' single-wafer processing systems for SiC should see a strong uptick in demand.

Though the semiconductor market is dominated by 300mm wafer size, the demand for ≤200mm SiC wafers is expected to grow significantly in the future driven by demand from end markets such as automotive and 5G. We believe that as substrate manufacturers build capacity to meet this demand, niche players serving these manufacturers such as RVS, will experience an uptick in demand for their products.

Throughput of batch systems diminishes dramatically with larger wafer sizes. At the same time, wafer manufacturers must meet tighter tolerances on wafer flatness, surface quality and wafer-to-wafer consistency that are difficult to achieve with batch processes.

The new kid on the block: Silicon Carbide (SiC)

Why Si substrates need an alternative

Si-based devices are reaching their performance limits due to continuing evolution of complex ICs and the following limitations of Si:

- Modern ICs uses electron holes where mobility is paramount. Holes are lack of an electron at a position in an atom, which leaves the particles net positively charged, allowing easy flow of current. Hole mobility in Si is very poor, resulting in a barrier for performance progression.
- Si's performance degrades in higher temperature. As circuits with multiple transistors heat up, Si-based devices need cooling support.
- Si is very poor at transmitting photons (light), depending on the photon wavelength. Consequently, alternative semiconductor compounds are required in lasers, LEDs and other photonic devices.

To overcome these constraints and enhance IC performance, alternative semiconductor compounds are being increasingly used in high-power products such as amplifiers and power transmission devices. A few of the alternative compounds gaining traction in the industry include SiC, GaN and Gallium Arsenide (GaAs).

SiC is becoming the material of choice for substrates

Wide bandgap semiconductor compounds, such as SiC, have superior properties

The semiconductor industry is increasingly adopting wide bandgap devices, which have a relatively high energy gap that allows devices to operate at higher voltages, frequencies and temperatures. SiC and GaN are preferred compounds for use in wide bandgap semiconductors owing to their superior conduction and switching (switching between various states) properties.

As a result, the SiC share in wafer manufacturing is expected to grow at a healthy rate with market research firm Yole estimating SiC's share in wafer manufacturing to grow from 2.7% in 2018 to 7.2% in 2023 (Figure 21).

Bandgap explained

Electronic bandgap is the energy gap between the conduction band and valence band. These bands relate to electron energy levels. Each band can hold a certain number of electrons. If an atom has more electrons, the extra electrons move to high energy bands. In the presence of an external energy source, equilibrium of electrons can be maintained within the material. Depending on the distribution of the energy bands, and the gap between them, different materials will have varied electrical properties. It is the bandgap that provides semiconductors the ability to switch currents on and off as desired in order to achieve a given electrical function (Figure 20).

Figure 20: Energy bandgap in materials

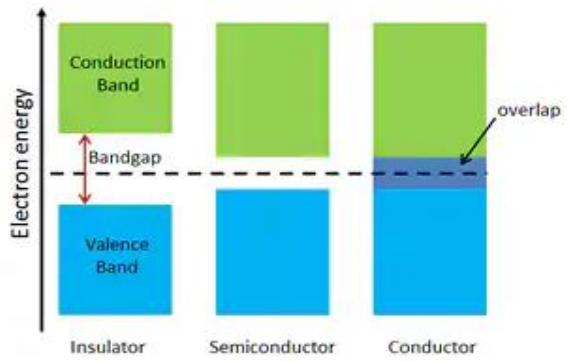
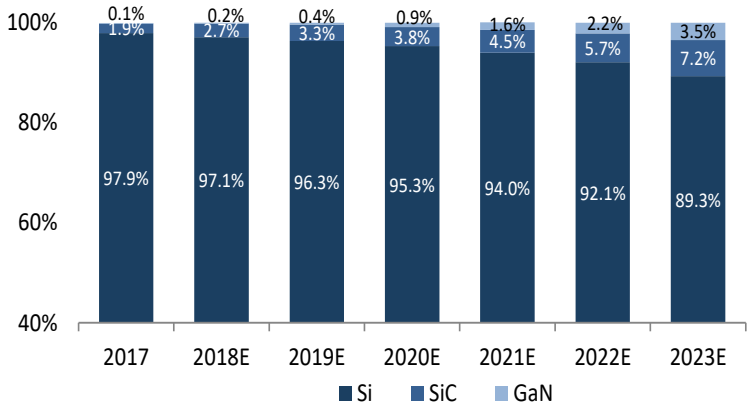


Figure 21: Share of materials in wafer manufacturing



Source: Mouser Electronics, Yole, Pitt Street Research

Compared to Si, SiC can sustain 10x higher voltage, has 3x higher thermal density and has 3x higher energy band

Compared to Si, SiC has several key advantages (Figure 22), including 3x wider bandgap, 3x thermal conductivity and 10x breakdown electric field strength.

Figure 22: Properties of SiC, Si, GaAs and GaN

Properties	Si	SiC	GaAs	GaN
Crystal Structure	Diamond	Hexagonal	Zincblende	Hexagonal
Energy Gap: E_G(eV)	1.12	3.26	1.43	3.5
Electron Mobility: μ_n(cm^2/V_s)	1,400	900	8,500	1,250
Hole Mobility: μ_p(cm^2)	600	100	400	200
Breakdown Field: E_B(V/cm)X10^6	0.3	3.0	0.4	3.0
Thermal Conductivity (W/cmK)	1.5	4.9	0.5	1.3
Relative Dielectric Constant: e_s	11.8	9.7	12.8	9.5

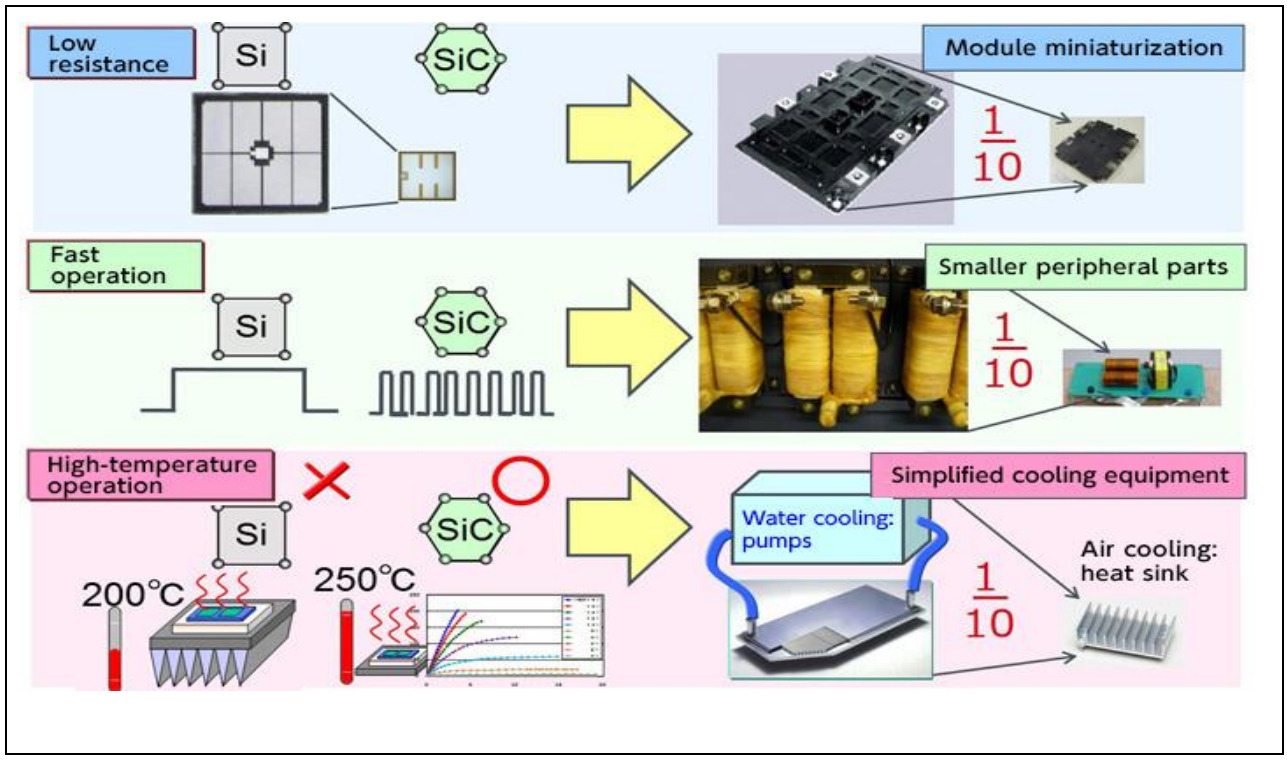
Source: ROHM, Pitt Street Research

- Electron Mobility – This specifies the speed of electron movement through a metal or semiconductor under the influence of an electric field. Higher electron mobility leads to better device performance.
- Hole Mobility – Hole mobility relates to the lack of an electron at a position in an atom, which leaves the particles net positively charged, allowing easy flow of current. With higher hole mobility, the ability to use electron holes for net positive charging in the circuit decreases and so a lower value is preferred for materials used in power management devices.
- Breakdown Field – This is a measurement relating to the ability of any material to sustain high voltages. High breakdown fields make a compound a strong candidate for use in ultrahigh voltage power devices.
- Thermal Conductivity – The ability of any material to conduct/transfer heat. A higher heat transfer capability per unit time is a prerequisite for any material to be used in high-power devices.
- Relative Dielectric Constant – This is the relative resistance of any material while forming an electric field in a vacuum. Materials with lower dielectric constant are favourable for high-power devices as they will lead to minimum electric power loss.

These properties of SiC lead to several benefits in terms of system performance (Figure 23) when compared to Si-based devices.

- **Higher voltages**: In electrical applications, heating is often an unwanted by-product of current flow. This diversion of energy is referred to as resistive loss. SiC, having the ability to sustain higher voltages, i.e., a high breakdown field, can be used to enable smaller devices with low resistive losses. Further, it can help reduce system complexity and cost, and improve reliability.
- **Higher conversion efficiency**: Devices made from SiC can switch currents relatively faster with less power loss. Also, it helps reduce the size of energy storage devices such as capacitors and inductors.
- **Higher currents**: SiC can carry much higher currents reducing the area of devices as well as the parasitic (or stray) capacitance.
- **Higher operating temperature and thermal conductivity**: SiC-enabled devices can operate well over 400 degree centigrade (vs. Si at 150 degree centigrade) and have a much higher thermal conductivity compared with Si. This improves the reliability of the device and also eliminates the need for ancillary components such as cooling systems, which provides significant reductions in cost and size.
- **Higher energy band gap**: SiC has a higher energy band gap than Si making it more robust against disturbance such as heat, radiation or electromagnetic fields. This makes it more suitable for sensor and military applications.

Figure 23: Benefits of SiC over Si



Source: Tech Web, ROHM, Pitt Street Research

In summary, SiC can produce smaller, faster, cheaper and more efficient devices, with the ability to operate at higher voltages, temperatures and frequencies. In addition, it also produces devices with greater durability and reliability. Consequently, SiC is likely to become the substrate of choice for high voltage power applications (EVs, charging infrastructure, solar power, wind power, data centres) and radio frequency devices.

SiC end market applications

SiC-based transistors possess several advantages over various varieties of Si-based transistors in terms of rated voltage (higher), speed (higher) and ON-resistance (lower). These properties make SiC-based substrates the preferred choice for the following applications:

- **EVs, industrial motors and traction inverters:** SiC-based power semiconductors are used in the onboard charging units in EVs and it is also making inroads in a key part of the system – the traction inverter – which provides pull to the motor in order to propel a vehicle.

  Tesla is using SiC-based MOSFET for its Model 3 inverter

  SiC-based power modules eliminate switching losses, which enable fast switching and significantly improve the low torque motor efficiency. High switching frequency also reduces motor copper and iron losses. Specifically, for EVs, this results in an efficiency increase of 5-12%. For instance, Tesla has been integrating SiC MOSFET-based (metal-oxide-semiconductor field-effect transistor) power modules from STMicroelectronics in its Model 3 inverter.

- **Solar/PV cells:** Compared to Si, SiC saves 10 megawatts (MW) for each gigawatt (GW) installed per year and 500 watts for every second in operation. Due to the better physical properties of SiC (as compared with Si) it provides several advantages for PV cells, such as;
  - High junction temperature[2] capability allowing the heat sink[3] to be small and light to increase the power density of PV inverters.
  - A low dielectric constant allows low parasitic capacitance and fast switching frequency, which in turn allows reduction of weight and volume of PV inverters.
- High critical electric field allows reduction of ON-resistance[4] and junction capacitance[5] while improving switching frequency and reducing conduction loss.
- **RF and 5G equipment:** Both SiC and GaN possess superior properties compared to Si for RF (radio frequency) devices. SiC is a superior semiconductor because of its higher bandgap and thermal conductivity than GaN or Si implying that SiC-based devices can operate at higher power densities than GaN or Si.

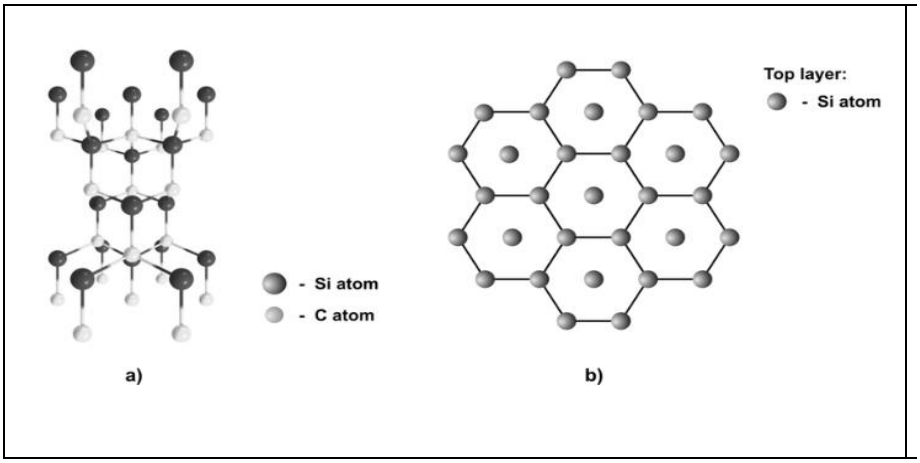
  SiC's superior electron mobility and thermal conductivity make it highly suitable for RF and 5G applications

  In either case, the devices of interest for switching and RF power applications require an epitaxial layer (elaborated in next section) of either SiC or GaN to be grown or deposited on a substrate composed of either the same (homoepitaxy) or a different (heteroepitaxy) material. Thus, considering all this, heteroepitaxial GaN on SiC is best suited for telecom and wireless applications due to the following key characteristics:

[2] Junction temperature refers to the highest operating temperature of the semiconductor in an electronic device.
[3] Heat sink is a thermal conductive metal device designed to absorb and disperse heat away from high temperature objects such as computer processors.
[4] ON-resistance is the resistance value between the Drain and Source of a MOSFET; a lower value signifies lower power loss.
[5] Junction capacitance is the capacitance associated with the charge variation in the depletion layer (of a p-n diode). A higher value adversely impacts the performance of high-speed or high-frequency circuits.

- As in other application areas, the high thermal conductivity of SiC-based devices allows them to run at a much higher voltages while the higher power density increases efficiency of the overall wireless infrastructure.
- The cubic crystalline lattice structure of SiC (Figure 24) allows a region of bandgap change to be formed without changing the structure of the substrate material and hence, lowering the defect density, which improves the reliability.

Figure 24: Lattice structure of SiC



Note: a) Fragment of 3C-SiC crystal lattice; b) Top layer structure of the surface

Source: Research Gate, Pitt Street Research

Strategic importance of SiC to the industry

While Si is currently still the most used material in 200mm wafer manufacturing, it is expected that SiC will gradually become the material of choice at least for RF and power devices on ≤200mm wafers.

Cree, a vertically integrated supplier that produces SiC wafers as well as power semiconductors, RF devices and LEDs, is the market leader in SiC substrate manufacturing (Figure 25). SiCrystal, II-IV Inc., Dow Corning and Showa Denko are other key players in this space.

Some IDMs, such as STMicroelectronics (see below), have started to integrate backwards in order to secure the supply of SiC wafers. With the increasing adoption of SiC wafers, especially in EV, PV and power management applications, we believe that RVS is poised to benefit significantly.

Figure 25: SiC-based substrate manufacturers

SiC Supplier
Cree
SiCrystal
II-IV
Dow Corning
Showa Denko
Others

Source: Wafer Works, Pitt Street Research

In response to the anticipated increase in demand for SiC-based semiconductors, IDMs are adding manufacturing capacity. Some of the key initiatives include:

- **Cree's US$1bn SiC expansion plans:** In May 2019, Cree announced that over the next five years, the company will invest US$1bn to expand its SiC and GaN capacity. Notably, of the total investment, Cree plans on deploying US$450m to create a dedicated automotive wafer fab for producing 200mm SiC wafers.
- **Cree's strategic shift towards Wolfspeed business**: From planning on selling the Wolfspeed business (engaged in providing SiC and GaN-based power and RF solutions) to Infineon back in 2016, Cree has switched its strategy driven by the growth in demand for SiC and GaN chips. In May 2019, Cree announced the sale of its Lighting Products business to Ideal Industries Inc., and plans on using the proceeds from that sale to expand its Wolfspeed business.
- **STMicroelectronics and Norstel AB:** In February 2019, to control its supply chain for SiC substrates, STMicroelectronics acquired a majority stake in Swedish SiC substrate manufacturer, Norstel AB for ~US$138m, with the former having an option to acquire the remaining 45% shares.
- **STMicroelectronics and Cree**: In January 2019, in order to secure its supply for SiC wafers, STM signed a multi-year agreement with Cree, whereby the latter will supply US$250m worth of 150mm SiC bare and epitaxial wafers to STM.
- **Infineon's acquisition of Siltectra**: In order to ramp up its production of SiC-based products, Infineon acquired Siltectra GmbH for EUR124m in November 2018. The rationale behind the acquisition was to acquire

Siltectra's Cold Split technology for creating individual SiC wafers from ingots, enabling a higher production volume of SiC wafers.

- **Cree's acquisition of Infineon's RF business:** In March 2018, in order to expand its market share in the GaN-on-SiC RF business segment, Cree acquired Infineon's RF business, that targets the wireless infrastructure industry, for EUR345m.
- **Horizon 2020**: As part of the European Commission's Horizon 2020 goal to ensure the global competitiveness of the region, the Commission plans to build the world's first pilot production facility to produce power electronics based on 200mm SiC chips. In order to achieve this goal, the Commission has signed on II-VI Inc. to supply 200mm SiC substrates under REACTION, a four-year programme under Horizon 2020, which will be funded by the EU.

Challenges for adoption of SiC in volume-centric products

Despite many advantageous properties, there are certain limitations of SiC usage in relation to high volume production.

- Production Cost: SiC is not a natural mineral, but a compound. It requires heavy furnace technology/investment to produce the compound from Si. The high production costs can be a limiting factor for smaller companies and may inhibit adoption of certain SiC-based ICs.
- Packaging Cost: For SiC-based devices to perform at the highest potential, the substrate used as packing module needs to have high voltage insulation and strong thermal management, and it also needs to be specifically designed. This may inhibit growth of SiC-based devices as IDMs are required to make additional investment in upgrading manufacturing facilities, exclusively for the packing module of the devices. The higher manufacturing costs can limit the attractiveness of SiC-based devices for certain lower end application areas.

While Si is currently still the most used material in 200mm wafer manufacturing, SiC is becoming strategically important due to its superior thermal conductivity and power handling capabilities. With substrate manufacturers competing to secure enough supply of SiC wafers, this provides a promising outlook for RVS which is primarily targeting the ≤200mm SiC wafer manufacturers.

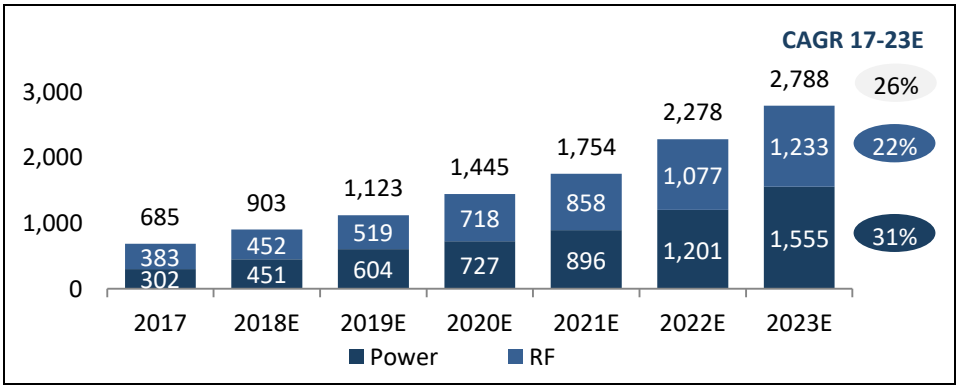
Large opportunity for SiC device manufacturers

Si is expected to remain the dominant material for substrate manufacturing in the near future. However, due to its better electrical qualities, SiC is making its way into high-performance and higher-priced power electronics applications – especially in photovoltaic (PV) inverts, EVs and hybrid electric vehicles (HEVs), as well as charging infrastructure.

SiC device market for power and RF is anticipated to grow at a 26% CAGR through 2023

The SiC device market is expected to grow exponentially in the next few years, with increasing demand from underlying end markets. Market research firm Yole estimates the SiC device market for power and RF applications (excluding communications applications) to grow at a 26% CAGR between 2017 and 2023 (Figure 26).

Figure 26: SiC device market for power and RF applications (US$m)



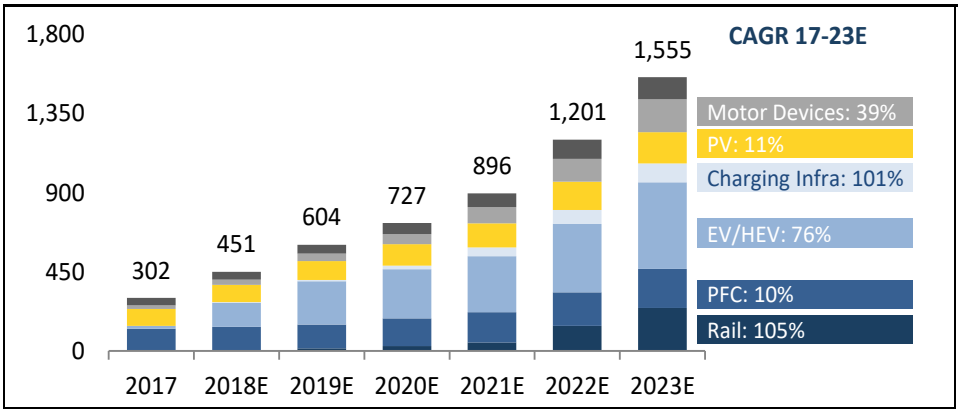
Source: Yole, SiC Device Market Report 2017

EV ecosystem to charge SiC demand

SiC demand in the power segment is currently driven primarily by the power factor correction (PFC) and PV markets. However, in the next five years, the main drivers for SiC are expected to be EVs/HEVs, charging infrastructure and rail. Yole estimates the SiC power device market to grow at a significant CAGR of 31%, from US$302m in 2017 to US$1.56bn in 2023 (Figure 27), with a major contribution from the EV ecosystem (EVs/HEVs and charging infrastructure).

EV/HEV and charging infrastructure to be the key end markets for SiC power devices

Figure 27: SiC power device market – by application (US$m)

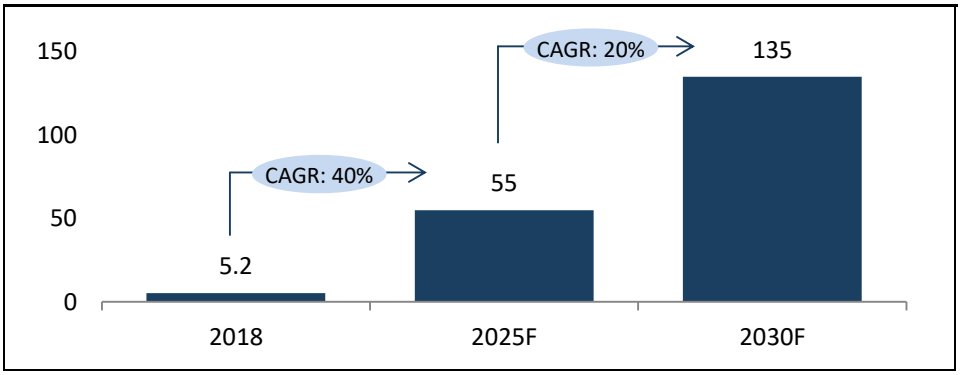


Source: Yole, SiC Device Market Report 2017, Pitt Street Research

Faster adoption of EVs/HEVs driven by regulation

The automotive industry, including global road transport, contributes ~17% of the global greenhouse gases. Consequently, many countries have pledged to move away from the production of internal combustion engines. In order to encourage the use of cleaner mobility (such as EVs/HEVs), various governments are introducing favourable regulations such as tax rebates, access to priority lanes, free parking and free electricity. This is expected to result in a rapid expansion in the number of EVs. The International Energy Agency (IEA) estimates the global stock of electric passenger cars to reach 55 million by 2025 and 135 million by 2030, growing 31% on average per year between 2018 and 2030 (Figure 28).

Figure 28: Global number of electric passenger cars (million)



Source: IEA, OECD

SiC devices are the preferred choice of EV manufacturers due to the favourable electric properties, e.g., longer battery life and driving range, faster charging, cheaper and lighter weight. Consequently, demand for SiC-based ICs is bound to post a rise.

SiC power management devices for EVs are anticipated to grow at 76% CAGR through 2023

Along with the increase in the number of plug-in EVs, the number of SiC devices used per vehicle is also expected to post an uptick due to the need for additional features, such as advanced sensing, connectivity, analytics and alert solutions in vehicles. Yole estimates the SiC power device market for EVs/HEVs to grow at a staggering CAGR of 76% between 2017 and 2023.

The need for charging infrastructure to grow in tandem

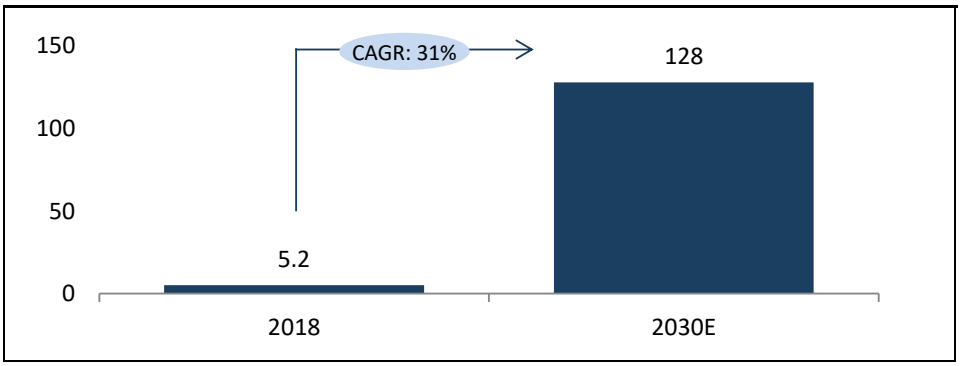
With the faster adoption of EVs/HEVs, demand for high-power charging infrastructure – another end market for SiC chips – will also increase. According to the IEA, the total number of electric light-duty vehicle chargers is expected to grow to 128 million by 2030, up from ~5 million in 2018 (Figure 29).

SiC ICs for charging infrastructure to double each year through 2025

SiC chips are preferred in high-power fast chargers that use direct-current fast charging (DCFC) technology to convert AC from the grid to DC before it enters the vehicle. Moreover, new technologies are being developed using SiC semiconductors to make the chargers more efficient. In late 2018, researchers at the North Carolina State University built an EV fast charger (using medium-voltage fast-charge technology, deploying SiC semiconductors) that is at least 10x smaller than existing systems and wastes 60% less power during the charging process, without sacrificing the charging time.

The increasing usage of SiC semiconductors in charging infrastructure is reflected in the expected market size of this application – Yole estimates the market to grow at an astounding CAGR of 101% from 2017 to 2025.

Figure 29: Number of light-duty vehicle chargers (million)



Source: IEA, OECD

SiC-based power electronic systems to drive the 5G revolution

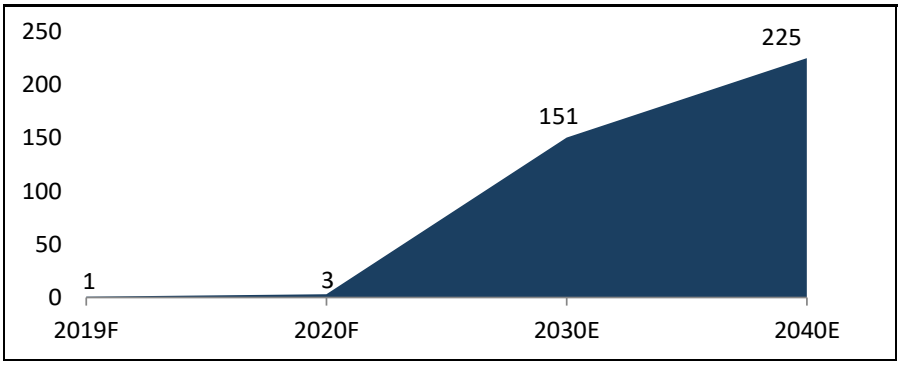
SiC demand will grow with increase in 5G infrastructure spending

The growing usage of devices that require faster processing speed and lower latency – such as video, augmented reality and virtual reality applications for gaming, shopping, autonomous vehicles and unmanned aerial vehicles – has resulted in the need for faster wireless communications networks, i.e., 5G.

5G propagates less than 4G over a long distance as it operates at higher frequencies. As a result, there is a need to upgrade networks and build more cellular base stations. Market research firm Frost and Sullivan expects that by 2025, there will be 1.2 billion 5G connections globally, accounting for 14% of all mobile connections (excluding cellular IoT). It also estimates that an investment of US$150bn will be required on 5G infrastructure by 2030 and US$225bn by 2040, to meet global demand (Figure 30).

Previously, Si-based devices were used in cellular base stations that supported 4G networks; however, their inability to perform at higher frequencies, higher voltage and higher temperatures will pave way for the adoption of SiC-based semiconductors for 5G networks. Moreover, SiC has become the preferred choice for 5G infrastructure based on its lifetime total cost of ownership.

Figure 30: 5G infrastructure spending (US$bn)



Source: Frost & Sullivan, End-markets for Semiconductor Manufacturing Equipment

SiC, due to its superior electrical properties, has carved its way into the high-priced power electronics applications, especially for EV and 5G infrastructure. RVS, the dominant player in the SiC grinding market, foresees a large addressable market that is expected to take off.

Revenue growth driven by new products

RVS currently has two new products in the pipeline – a new SiC polisher (commercial launch expected in 2HY19) and a CMP system (anticipated launch in 2020). We believe that the introduction of these new products provides RVS with substantial potential for revenue growth in the short-to-medium term.

The new SiC polisher will allow RVS to tap into the rapidly growing end markets for electric vehicles and 5G wireless infrastructure. In our view, RVS' sales will grow in tandem with these markets as the company expands its customer base.

Furthermore, the new system is expected to sell for ~2x RVS' current ASP. As per our estimates, this should bring the blended ASP to ~US$800k in FY20, ~24% higher than the blended ASP of US$645k in FY17–18.

Additionally, we expect there to be a significantly larger impact on the ASP and gross margin as the shipped volumes increase FY20 onwards. Once shipments of both the SiC polisher and the new CMP system start growing, the blended ASP should increase substantially to ~US$950k and ~US$1,132k in FY21 and FY22, respectively.

Higher ASP and gross margins from new products to drive revenues and earnings

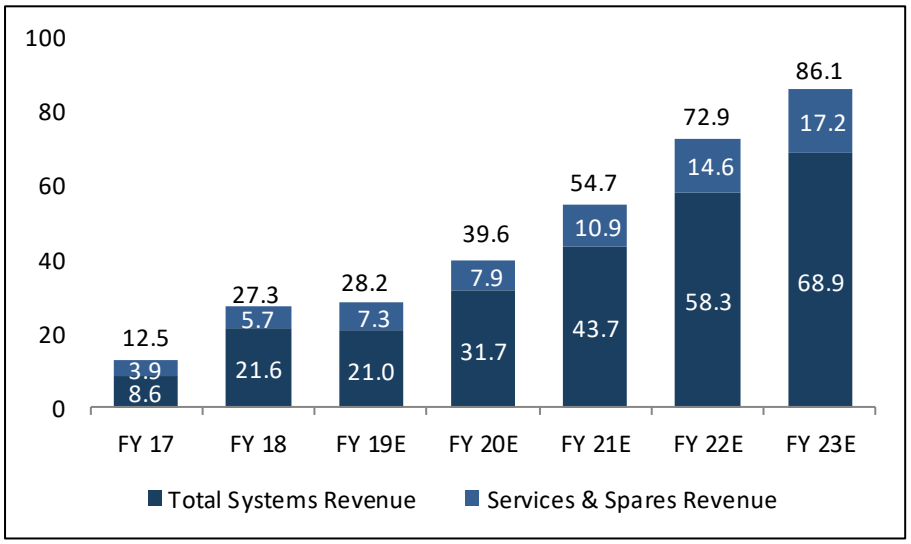
Consequently, RVS' bottom line will benefit from higher gross margins, allowing the company to become profitable in FY20. We have maintained a conservative outlook on the commercial launch of CMP systems for the 300mm wafer size, which RVS expects to launch in another 2–3 years. Potential revenues from CMP systems have not been factored in our earnings estimates.

RVS has been successfully expanding its customer base, as evidenced by the addition of 7 new customers in FY18. This is expected to provide the company additional opportunity to cross-sell the new machines, supporting revenue growth.

Moreover, as more machines are sold, there will be incremental requirement for spare parts and support services, which should further contribute to revenue growth.

Based on the above, we forecast RVS' total revenue to grow at a 5-year CAGR of 26%, reaching US$86.1m in FY23, from US$27.3m in FY18 (Figure 31).

Figure 31: Revenue growth trajectory (US$m)



Source: Pitt Street Research

RVS on track to become profitable in FY2020

Gross margins are projected to expand, primarily driven by a favourable product mix and better operating leverage. RVS is targeting a gross margin of 45–47% in the medium term, broadly in line with the semiconductor equipment peer group.

The upcoming new products, such as the new SiC polisher, should command higher ASPs and gross margins than the existing product portfolio.

~50% gross margins on spare parts and support services

Moreover, driven by the sharp growth in system sales and increasing age of the installed base, the usage of spare parts and support services is expected to rise proportionately. In our view, this would substantially contribute to higher blended margins, as spare parts and services enjoy a healthy gross margin of ~50%.

RVS is also expected to derive cost reduction benefits from outsourcing manufacturing of some fabricated metal components to Zhejiang Jingsheng, its manufacturing and distribution partner in China for certain legacy products.

Further, the company plans to shift its operating model – shipping subsystems directly to the client's site and conducting assembly and testing services on-site to reduce assembly and configuration costs and time.

We believe the effects of higher gross margins and cost reductions will drive profitability over the next few years. We expect EBITDA margins to expand substantially from 3.0% in FY18 towards 24% by FY22 (Figure 32). While RVS attained breakeven at the EBITDA level (on an adjusted basis, considering the share-based compensation expense and IPO costs) in FY18, the company is on track to be net positive by FY2020.

Figure 32: Gross margin on the rise for RVS

Margins (%)	2017A	2018A	2019F	2020F	2021F	2022F	2023F
Gross margins	31.9%	37.3%	31.2%	39.5%	42.6%	44.5%	46.3%
EBITDA margin	-25.0%	3.0%	-8.7%	10.2%	18.1%	23.8%	27.9%
EBIT margin	-28.7%	1.9%	-12.4%	7.2%	15.1%	20.8%	24.9%
Adj. attributable profit margin	-30.0%	-0.1%	-15.0%	5.2%	13.2%	17.0%	18.4%

Source: Pitt Street Research

IPO proceeds to support growth plans

Following the completion of its IPO in early December 2018, RVS' net cash balance expanded 10x, from US$2.4m in 2017 to US$24.5m in FY2018. In our view, this strong cash position will fuel the company's expansion plans by enabling it to continue to innovate.

RVS is currently developing its first SiC polisher, with inputs from key customers, and also has a new CMP system in the pipeline to expand its foothold in the Si device applications market. We believe that with a strong balance sheet (with ~80% funding by equity and negligible debt), the company is well-funded to meet its near to medium term R&D needs.

In our opinion, the substantial cash balance also allows for the possibility of bolt-on acquisitions to strengthen RVS' technological base.

Valuation implies significant upside potential

In order to derive RVS' long-term value, we have used a weighted average valuation methodology, assigning equal weights to a peer-group-based relative valuation and a discounted cash flow (DCF) calculation.

To arrive at a relative valuation, we have considered various companies that operate in this space (Figure 33), including ASX-listed Pivotal Systems and major players in Japan – DISCO Corp, Ebara Corp, Tokyo Seimitsu, Horiba and Okamoto Machine Tool Works. Some major global players, including Applied Materials, ASM International, Lam Research and KLA-Tencor Corp have also been included in the peer-group.

Figure 33: Peer group valuation

Company Name	Ticker	P/BV
		FY2020
Pivotal Systems	ASX:PVS	NA
Applied Materials	NasdaqGS:AMAT	5.2x
ASM International	ENXTAM:ASM	2.0x
Lam Research	NasdaqGS:LRCX	6.2x
Disco Corporation	TSE:6146	3.1x
Ebara Corporation	TSE:6361	0.8x
Tokyo Seimitsu	TSE:7729	1.1x
HORIBA	TSE:6856	1.2x
Okamoto Machine Tool Works	TSE:6125	NA
KLA-Tencor Corporation	NasdaqGS:KLAC	8.3x
Average		**3.5x**

Source: S&P Capital IQ, Pitt Street Research

Taking the peer average P/BV multiple of 3.5x and applying it to RVS' forecasted book value for FY20 yields an equity value of A$2.34 per share under our base case scenario (Figure 34).

Industry going through a cyclical downturn, depressing multiples

The current cyclical downturn has depressed valuation multiples. Strong multiple expansion is expected when industry goes back into expansion mode

We would argue that the semiconductor industry is currently going through a cyclical downturn, depressing valuation multiples, such as P/B, which has traditionally been our preferred valuation metric for semiconductor equipment companies. P/B can typically expand to ≥ 4x during upcycles.

In other words, when semiconductor industry fundamentals turn the corner, as they always have in the past, we expect strong multiple expansion throughout the industry, including RVS'.

This expansion would drive RVS' valuation substantially higher as we will discuss in our bull case scenario below.

Figure 34: Relative valuation per share (base case)

Equity value determination (USDm unless specified otherwise)	P/ BV
Sector Average Multiple	3.5x
Discount/ Premium	0.0%
Equity/Book value	**34.6**
Diluted Shares (m)	77
Implied price (USD)	1.57
Exchange Rate	1.49
Implied price (AUD)	**2.34**
Current price (AUD)	1.49
Upside (%)	56.8%

Source: Pitt Street Research

DCF calculations suggest value of A$2.27 per share

Our DCF model yields a WACC of 11.9% for RVS (risk-free rate of 1.9%, a beta of 1.2 and an equity risk premium of 8.5%). Applying this discount rate to our free cash flow projections through FY28E, coupled with a terminal growth rate of 2%, yields a value of A$2.27 per share for RVS (Figure 35).

Figure 35: DCF value in A$ using various WACCs

Sensitivity Analysis									
WACC	**11.9%**								
Terminal Growth Rate	**2.00%**	**Change in WACC**							
		11.2%	*11.4%*	*11.7%*	*11.9%*	*12.2%*	*12.4%*	*12.7%*	*12.9%*
	1.25%	2.38	2.30	2.23	2.16	2.10	2.03	1.97	1.92
	1.50%	2.42	2.34	2.27	2.19	2.13	2.06	2.00	1.94
	1.75%	2.46	2.38	2.30	2.23	2.16	2.09	2.03	1.97
Terminal Growth Rate	*2.00%*	2.51	2.42	2.34	**2.27**	2.19	2.13	2.06	2.00
	2.25%	2.56	2.47	2.38	2.30	2.23	2.16	2.09	2.03
	2.50%	2.61	2.51	2.43	2.34	2.27	2.19	2.12	2.06
	2.75%	2.66	2.56	2.47	2.39	2.31	2.23	2.16	2.09

Source: Pitt Street Research

In our view, as RVS introduces new products in the SiC segment, as well as branches out into the CMP market, it will have access to a broader customer base in terms of end applications, providing it potential for lower discount rates.

Moreover, new product launches will provide RVS the base to further expand its range of offerings. For instance, the new 200mm CMP machine has the potential of being upgraded for 300mm wafer sizes in the next 2–3 years. We believe that this transition may translate into further share price increases going forward.

Fair value of A$2.30 in base case

Our fair value of A$2.30 per share has been derived from a weighted average valuation methodology, where we assigned equal weights to the relative valuation and our DCF calculation (Figure 36).

Figure 36: Weighted average valuation in our base case scenario

Methodology	Weight (%)	Share price (AUD)
DCF	50.0%	2.27
Relative valuation	50.0%	2.34
Composite		**2.30**
Current Price		1.49
Upside/ Downside (%)		**54.6%**

Source: Pitt Street Research

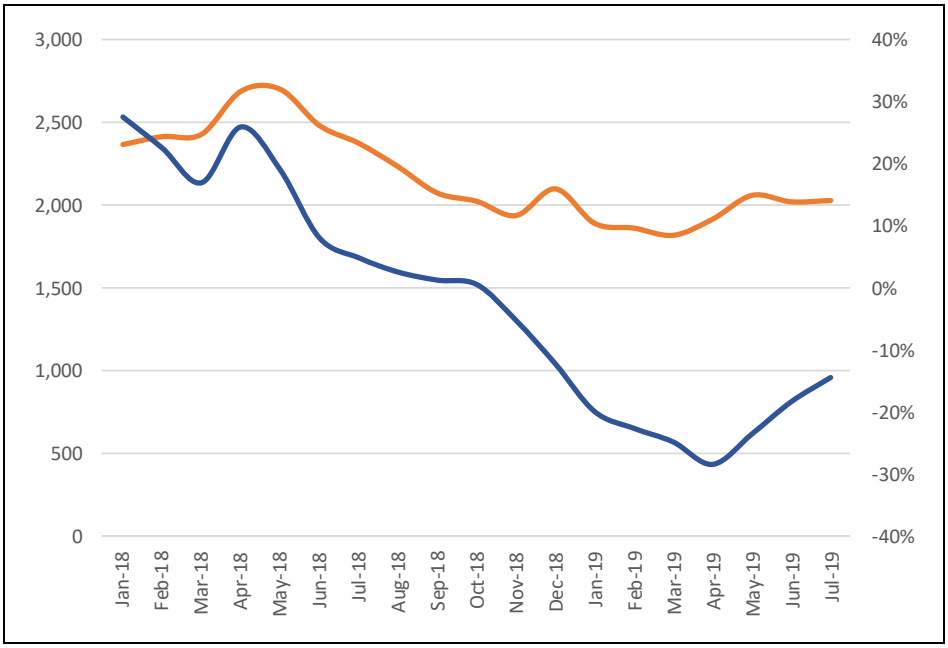
Bull case: Cyclical upswing to drive multiple expansion

Cyclical upswing may already be underway

While we are not taking a view on the timing of a cyclical recovery of the semiconductor industry, and hence the semiconductor equipment market, we do believe that when this recovery kicks in, we are likely to see strong multiple expansion for equipment companies.

The most recent statistics from SEMI regarding North American semiconductor billings (Figure 37) indicates lower year-on-year declines in May 2019. This may imply that the cyclical recovery has already started. Case in point, in its most recent earnings call, Micron Technology Inc. (NASDAQ:MU), one of the world's largest DRAM manufacturers, forecasted a "healthy" year-on-year revenue growth in the second half of calendar 2019.

Figure 37: Y-o-Y growth in North American semiconductor equipment billings



Source: SEMI, Pitt Street Research

Bull case valuation of A$ 2.69 per share

As stated earlier, when the cyclical recovery sets in, we expect to see strong multiple expansion across the industry. On a P/B basis, we believe an industry average of 4x is a reasonably modest target.

Applying this to our estimated book value for RVS of US$34.6m in FY20 yields a value of A$2.69 of per share.

Conclusion: Making all the right moves

RVS' strategy to expand its product portfolio on the basis of end applications provides it with substantial growth potential, in our view. To date, RVS has largely been addressing the substrate manufacturing segment. However, the introduction of RVS' new CMP system will allow the company to expand its addressable market.

Moreover, the new SiC polisher allows RVS to tap high-growth end markets, such as automotive and 5G, on the back of SiC's growing acceptance among IDMs as the substrate of choice in these end markets.

We believe the benefits from these initiatives, coupled with transition towards a higher blended ASP, contribute to a potential re-rating of the company's stock.

Our valuation range for RVS is A$2.30 to A$2.69 per share.

Risks

In our view, there are four main risks associated with investing in RVS:

1. Reliance on key clients: RVS' top 5 customers accounted for 88% of its total revenue in FY2017. However, with the addition of 7 new customers in FY18, this figure was significantly reduced to 61% (as of December 2018). We believe that with the on-boarding of new customers, following the introduction of the new SiC polishing system, RVS' customer portfolio will become more diversified.
2. Order delays: In its recent earnings release, RVS revised its revenue guidance to reflect order delays from one of its customers. In our opinion, customer deposits paid on order confirmation provide assurance that orders, although delayed, will be shipped.
3. Cyclicality: The memory and storage markets, specifically DRAM and NAND Flash, are highly cyclical. However, we believe that RVS' current initiatives to grow in the SiC domain provide it with good buffer against cyclicality in the Si markets.
4. Execution risk: As RVS introduces its new SiC polisher, and as it enters the mainstream CMP market with its new product offering, there is a risk associated with the company's ability to manufacture new tools on time, given that substantial portions of these new tools will be outsourced to third parties.
5. The US–China trade war: RVS is an Australia-domiciled company. Its US base of operations may lead to restrictions on exports of high-technology products and components to China. It may also lead to tariffs on components the company imports from China, even though RVS has some flexibility in component sourcing.

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